

Hari Angepat · Derek Chiou · Eric S. Chung James C. Hoe

# FPGA-Accelerated Simulation of Computer System



# Fpga Accelerated Simulation Of Computer Systems Derek Chiou

Shaoshan Liu,Zishen Wan,Bo Yu,Yu Wang

#### Fpga Accelerated Simulation Of Computer Systems Derek Chiou:

FPGA-Accelerated Simulation of Computer Systems Hari Angepat, Derek Chiou, Eric S. Chung, James C. Hoe, 2014-07-01 To date the most common form of simulators of computer systems are software based running on standard computers One promising approach to improve simulation performance is to apply hardware specifically reconfigurable hardware in the form of field programmable gate arrays FPGAs This manuscript describes various approaches of using FPGAs to accelerate software implemented simulation of computer systems and selected simulators that incorporate those techniques More precisely we describe a simulation architecture taxonomy that incorporates a simulation architecture specifically designed for FPGA accelerated simulation survey the state of the art in FPGA accelerated simulation and describe in detail selected instances of the described techniques Table of Contents Preface Acknowledgments Introduction Simulator Background Accelerating Computer System Simulators with FPGAs Simulation Virtualization Categorizing FPGA based Simulators Conclusion Bibliography Authors Biographies Quantum Computer Systems Yongshan Ding, Frederic T. Chong, 2022-05-31 This book targets computer scientists and engineers who are familiar with concepts in classical computer systems but are curious to learn the general architecture of quantum computing systems. It gives a concise presentation of this new paradigm of computing from a computer systems point of view without assuming any background in quantum mechanics As such it is divided into two parts The first part of the book provides a gentle overview on the fundamental principles of the quantum theory and their implications for computing The second part is devoted to state of the art research in designing practical quantum programs building a scalable software systems stack and controlling quantum hardware components Most chapters end with a summary and an outlook for future directions This book celebrates the remarkable progress that scientists across disciplines have made in the past decades and reveals what roles computer scientists and engineers can play to enable practical scale quantum computing Space-Time Computing with Temporal Neural Networks James E. Smith, 2022-05-31 Understanding and implementing the brain s computational paradigm is the one true grand challenge facing computer researchers Not only are the brain s computational capabilities far beyond those of conventional computers its energy efficiency is truly remarkable This book written from the perspective of a computer designer and targeted at computer researchers is intended to give both background and lay out a course of action for studying the brain s computational paradigm It contains a mix of concepts and ideas drawn from computational neuroscience combined with those of the author As background relevant biological features are described in terms of their computational and communication properties The brain s neocortex is constructed of massively interconnected neurons that compute and communicate via voltage spikes and a strong argument can be made that precise spike timing is an essential element of the paradigm Drawing from the biological features a mathematics based computational paradigm is constructed The key feature is spiking neurons that perform communication and processing in space time with emphasis on time In these paradigms time

is used as a freely available resource for both communication and computation Neuron models are first discussed in general and one is chosen for detailed development Using the model single neuron computation is first explored Neuron inputs are encoded as spike patterns and the neuron is trained to identify input pattern similarities Individual neurons are building blocks for constructing larger ensembles referred to as columns These columns are trained in an unsupervised manner and operate collectively to perform the basic cognitive function of pattern clustering Similar input patterns are mapped to a much smaller set of similar output patterns thereby dividing the input patterns into identifiable clusters Larger cognitive systems are formed by combining columns into a hierarchical architecture These higher level architectures are the subject of ongoing study and progress to date is described in detail in later chapters Simulation plays a major role in model development and the simulation infrastructure developed by the author is described Customizable Computing Yu-Ting Chen, Jason Cong, Michael Gill, Glenn Reinman, Bingjun Xiao, 2022-05-31 Since the end of Dennard scaling in the early 2000s improving the energy efficiency of computation has been the main concern of the research community and industry The large energy efficiency gap between general purpose processors and application specific integrated circuits ASICs motivates the exploration of customizable architectures where one can adapt the architecture to the workload In this Synthesis lecture we present an overview and introduction of the recent developments on energy efficient customizable architectures including customizable cores and accelerators on chip memory customization and interconnect optimization In addition to a discussion of the general techniques and classification of different approaches used in each area we also highlight and illustrate some of the most successful design examples in each category and discuss their impact on performance and energy efficiency We hope that this work captures the state of the art research and development on customizable architectures and serves as a useful reference basis for further research design and implementation for large scale deployment in future computing Robotic Computing on FPGAs Shaoshan Liu, Zishen Wan, Bo Yu, Yu Wang, 2022-05-31 This book provides a systems thorough overview of the state of the art field programmable gate array FPGA based robotic computing accelerator designs and summarizes their adopted optimized techniques This book consists of ten chapters delving into the details of how FPGAs have been utilized in robotic perception localization planning and multi robot collaboration tasks In addition to individual robotic tasks this book provides detailed descriptions of how FPGAs have been used in robotic products including commercial In-/Near-Memory Computing Daichi Fujiki, Xiaowei Wang, Arun autonomous vehicles and space exploration robots Subramaniyan, Reetuparna Das, 2021-08-12 This book provides a structured introduction of the key concepts and techniques that enable in near memory computing For decades processing in memory or near memory computing has been attracting growing interest due to its potential to break the memory wall Near memory computing moves compute logic near the memory and thereby reduces data movement Recent work has also shown that certain memories can morph themselves into compute units by exploiting the physical properties of the memory cells enabling in situ computing in the memory array

While in and near memory computing can circumvent overheads related to data movement it comes at the cost of restricted flexibility of data representation and computation design challenges of compute capable memories and difficulty in system and software integration Therefore wide deployment of in near memory computing cannot be accomplished without techniques that enable efficient mapping of data intensive applications to such devices without sacrificing accuracy or increasing hardware costs excessively This book describes various memory substrates amenable to in and near memory computing architectural approaches for designing efficient and reliable computing devices and opportunities for in near memory acceleration of different classes of applications Innovations in the Memory System Rajeev Balasubramonian, 2019-09-10 This is a tour through recent and prominent works regarding new DRAM chip designs and technologies near data processing approaches new memory channel architectures techniques to tolerate the overheads of refresh and fault tolerance security attacks and mitigations and memory scheduling The memory system will soon be a hub for future innovation While conventional memory systems focused primarily on high density other memory system metrics like energy security and reliability are grabbing modern research headlines With processor performance stagnating it is also time to consider new programming models that move some application computations into the memory system This in turn will lead to feature rich memory systems with new interfaces The past decade has seen a number of memory system innovations that point to this future where the memory system will be much more than dense rows of unintelligent bits

Address Space Translation for FPGA Accelerated Simulators Michael Thaddeus Chamberlain, 2015 FPGA 2008 .2008 Microarchitectural simulation is needed to help explore the large design space of new computer systems These simulations are taking increasingly longer amounts of time to run due to the increasing complexity of modern processors Co simulation and high level synthesis are promising fields to improve the overall time required for microarchitectural simulators and can contribute to low design times and fast simulation speeds permitting a larger range of design space exploration While promising co simulation techniques must find effective ways to map the host memory address space to the FPGA memory address space to be able to correctly transfer simulation data between the host and FPGA **FPGA Based Accelerators** for Financial Applications Christian De Schryver, 2015-07-30 This book covers the latest approaches and results from reconfigurable computing architectures employed in the finance domain So called field programmable gate arrays FPGAs have already shown to outperform standard CPU and GPU based computing architectures by far saving up to 99% of energy depending on the compute tasks Renowned authors from financial mathematics computer architecture and finance business introduce the readers into today s challenges in finance IT illustrate the most advanced approaches and use cases and present currently known methodologies for integrating FPGAs in finance systems together with latest results The complete algorithm to hardware flow is covered holistically so this book serves as a hands on guide for IT managers researchers and quants programmers who think about integrating FPGAs into their current IT systems **Fpga-Accelerated Analytics** 

Zsolt István, Kaan Kara, David Sidler, 2020-09-28 Datacenters hosting the data intensive applications used in machine learning and online services are facing an important challenge the amount of data that needs to be stored and processed is increasing at an exponential rate whereas traditional processor performance has been stagnating for years as Moore's Law tapers off Driven by these trends data processing and management applications have become increasingly distributed leading to new data movement bottlenecks at various levels of the software and hardware architecture The authors show how specialized hardware accelerators can provide an answer to the compute stagnation problem and be helpful in reducing data movement bottlenecks by placing them in the right location within the computer architecture They concentrate on Field Programmable Gate Arrays FPGAs and show how they make it possible to express algorithms in ways that are fundamentally different from CPUs or GPUs Many major companies are using these accelerator techniques in their storage and processing offerings The authors discuss the benefits of using FPGAs in the context of analytical processing both as an accelerator within a single node database and as part of distributed data analytics pipelines. They present guidelines for accelerator design in both scenarios and examples of integration within full fledged Relational Databases They do so through the prism of recent research projects that explore how emerging compute intensive operations in databases can benefit from FPGAs Finally they highlight future research challenges in programmability and integration and cover architectural trends that are propelling the rapid adoption of accelerators in datacenters and the cloud The monograph provides researchers and practitioners a concise insight into how FPGAs can play an important role in designing modern data intensive computing systems Drawing on both theory and practical implementations the readers are brought quickly up to speed on a technique that will significantly improve a system s performance Reconfigurable Computing Scott Hauck, André DeHon, 2010-07-26 Reconfigurable Computing marks a revolutionary and hot topic that bridges the gap between the separate worlds of hardware and software design the key feature of reconfigurable computing is its groundbreaking ability to perform computations in hardware to increase performance while retaining the flexibility of a software solution Reconfigurable computers serve as affordable fast and accurate tools for developing designs ranging from single chip architectures to multi chip and embedded systems Scott Hauck and Andre DeHon have assembled a group of the key experts in the fields of both hardware and software computing to provide an introduction to the entire range of issues relating to reconfigurable computing FPGAs field programmable gate arrays act as the computing vehicles to implement this powerful technology Readers will be guided into adopting a completely new way of handling existing design concerns and be able to make use of the vast opportunities possible with reconfigurable logic in this rapidly evolving field Designed for both hardware and software programmers Views of reconfigurable programming beyond standard programming languages Broad set of case studies demonstrating how to use FPGAs in novel and efficient ways **FPGA Acceleration of Molecular Dynamics** Simulations Yongfeng Gu, 2008 Abstract While molecular dynamics simulations MD are a fundamental method for gaining

the understanding of chemical and biological systems their computational cost is extremely high Simulating macromolecules requires thousands of node hours and cell level systems remain altogether out of reach We address this issue by using an emerging mode of high performance computing that is based on configurable logic in the form of Field Programmable Gate Arrays FPGAs The problem is that while FPGAs have often delivered 100 fold speed ups per node over microprocessor based systems the applications have generally been limited to those with small regular kernels operating on low precision integer data types MD possesses neither We address this problem by creating an explicitly designed FPGA coprocessor that can be integrated into generic commercially available systems MD is an iterative technique the forces on each particle are computed then applied using the equations of motion We use standard partitioning by computing bonded forces motion updates and bookkeeping on the host while computing the remaining forces which dominate on the FPGA accelerator For the short range forces we combine the following cell lists systematically determined interpolation and precision handling of exclusion and support for models with large numbers of particles This has required new microarchitectures for the cell list processor and off chip memory controller and extensive experimentation to explore the design space to optimize precision interpolation order interpolation mode table sizes and simulation quality To perform efficient and accurate numerical computation on FPGA we created a novel arithmetic mode that is tuned for computing high order polynomial interpolation For the long range forces we use the multigrid method we show that this is an excellent match to FPGAs with the primary operations having a favorable systolic structure and taking advantage of the large number of independently addressable RAMs The significance of this work lies at several levels the 5x to 10x acceleration of MD production code while retaining simulation quality the turings of algorithms for the FPGA the system integration the new arithmetic mode the numerous novel microarchitectures and the methods for optimizing MD implementations on FPGAs FPGA-Based System Design Wayne Wolf, 2004-06-15 Everything FPGA designers need to know about FPGAs and VLSI Digital designs once built in custom silicon are increasingly implemented in field programmable gate arrays FPGAs Effective FPGA system design requires a strong understanding of VLSI issues and constraints and an understanding of the latest FPGA specific techniques In this book Princeton University s Wayne Wolf covers everything FPGA designers need to know about all these topics both the how and the why Wolf begins by introducing the essentials of VLSI fabrication circuits interconnects combinational and sequential logic design system architectures and more Next he demonstrates how to reflect this VLSI knowledge in a state of the art design methodology that leverages FPGA s most valuable characteristics while mitigating its limitations Coverage includes How VLSI characteristics affect FPGAs and FPGA based logic design How classical logic design techniques relate to FPGA based logic design Understanding FPGA fabrics the basic programmable structures of FPGAs Specifying and optimizing logic to address size speed and power consumption Verilog VHDL and software tools for optimizing logic and designs The structure of large digital systems including register transfer design methodology Building large scale platform and multi FPGA systems A start

to finish DSP case study addressing a wide range of design problems PRENTICE HALL Professional Technical Reference Upper Saddle River NJ 07458 www phptr com ISBN 0 13 142461 0 **Rapid Prototyping of Digital Systems** James O. Hamblen, Tyson S. Hall, Michael D. Furman, 2007-09-26 New to this edition is an introduction to embedded operating systems for SOPC designs Featuring four accelerated tutorials on the Quartus II and Nios II design environments this edition progresses from introductory programmable logic to full scale SOPC design integrating hardware implementation software development operating system support state of the art I O and IP cores This edition features Altera's new 7 1 Quartus II CAD and Nios II SOPC tools and includes projects for Altera's DE1 DE2 UP3 UP2 and UP1 FPGA development boards FPGA Programming in C David Pellerin, Scott Thibault, 2005 FPGA brings high performance applications to market quickly this book covers the many emerging platforms in a proven effective manner FPGA-accelerated pattern matching over streams of events Louis Woods, 2009 Data Processing on FPGAs Jens Teubner, Louis Woods, 2013-06-27 Roughly a decade ago power consumption and heat dissipation concerns forced the semiconductor industry to radically change its course shifting from sequential to parallel computing Unfortunately improving performance of applications has now become much more difficult than in the good old days of frequency scaling This is also affecting databases and data processing applications in general and has led to the popularity of so called data appliances specialized data processing engines where software and hardware are sold together in a closed box Field programmable gate arrays FPGAs increasingly play an important role in such systems FPGAs are attractive because the performance gains of specialized hardware can be significant while power consumption is much less than that of commodity processors On the other hand FPGAs are way more flexible than hard wired circuits ASICs and can be integrated into complex systems in many different ways e.g. directly in the network for a high frequency trading application This book gives an introduction to FPGA technology targeted at a database audience In the first few chapters we explain in detail the inner workings of FPGAs Then we discuss techniques and design patterns that help mapping algorithms to FPGA hardware so that the inherent parallelism of these devices can be leveraged in an optimal way Finally the book will illustrate a number of concrete examples that exploit different advantages of FPGAs for data processing Table of Contents Preface Introduction A Primer in Hardware Design FPGAs FPGA Programming Models Data Stream Processing Accelerated DB Operators Secure Data Processing Conclusions Bibliography Authors Biographies Index An FPGA Implementation of FDTD Codes for Reconfigurable High Performance Computing ,2004 Finite difference time domain FDTD codes are used in modeling RF signatures and electronic coupling Despite improvements in large scale modeling simulation codes and the acquisition of powerful high performance computing HPC platforms simulations of such scientific problems require still more powerful computers The advances in Field Programmable Gate Array FPGA chips and FPGA based co processor FPGA CP boards offer the potential for accelerating current and future HPC platforms Higher capacity FPGAs offer an opportunity for implementing floating point applications previously infeasible In

this thesis I have investigated the feasibility of using FPGA CP acceleration for FDTD simulation. The FDTD method has been chosen for this case study due to its simple computation kernel and abundant parallelism. A floating point solver for eletro magnetic simulation has been implemented Results achieved in this thesis demonstrate the feasibility of high throughput and a good circuit density through the use of architectural features like the 18 bit block multipliers provided by modern day FPGAs

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