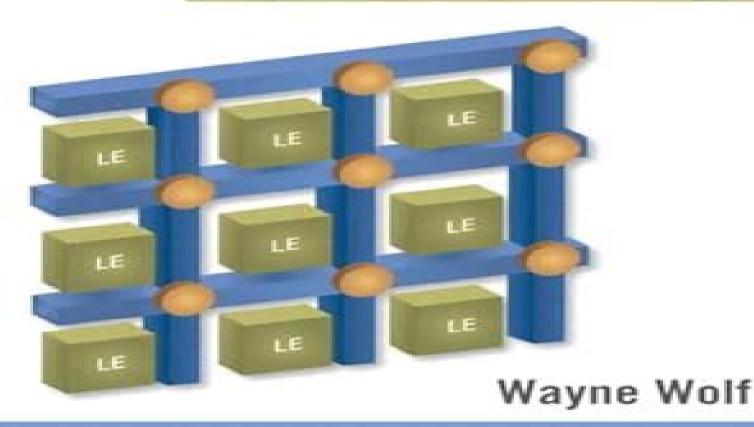


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Digital System Designs and others HDL based design has become an essential technique for modern digital systems This book focuses on developing verifying and synthesizing designs of practical digital systems using the most widely used hardware description Language Verilog HDL and FPGAs The main features of this book are Explains how to perform synthesis and verification to achieve optimized synthesis results and compiler times Offers complete coverage of Verilog HDL syntax Illustrates the entire design and verification flow using an FPGA case study Presents many real world worked design examples Gives readers deeper understanding with review questions in each section and end of chapter problems Emphasizes design implementation tradeoff options with coverage of ASICs and FPGAs **FPGA Design** Philip Andrew Simpson, 2015-05-19 This book describes best practices for successful FPGA design It is the result of the author's meetings with hundreds of customers on the challenges facing each of their FPGA design teams By gaining an understanding into their design environments processes what works and what does not work key areas of concern in implementing system designs have been identified and a recommended design methodology to overcome these challenges has been developed This book s content has a strong focus on design teams that are spread across sites The goal being to increase the productivity of FPGA design teams by establishing a common methodology across design teams enabling the exchange of design blocks across teams Coverage includes the complete FPGA design flow from the basics to advanced techniques This new edition has been enhanced to include new sections on System modeling embedded design and high level design The original sections on Design Environment RTL design and timing closure have all been expanded to include more up to date techniques as well as providing more extensive scripts and RTL code that can be reused by readers Presents complete field tested methodology for FPGA design focused on reuse across design teams Offers best practices for FPGA timing closure in system debug and board design Details techniques to resolve common pitfalls in designing with FPGAs

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