

Cryptographic Hardware & Embedded Systems for Communications

Nicolas Sklavos, *Member, IEEE*, Invited Speaker

Abstract— This work is related to System-On-A-Chip architectures and design methodologies, for cryptographic algorithms implementations. Alternative approaches are presented, for architecture and architectures for block ciphers, stream ciphers, and hash functions. The presented algorithms are the most wide used, in all certain of modern applications. Implementation aspects are given for both ASIC and FPGA integration platforms. Synthesis results are illustrated in hardware terms. This work also introduces the basic principles of random number generators, which are fundamental primitives of security applications also. Comparisons of operating frequency, throughput and allocated resources are given in detail. Future directions in hardware and embedded systems design, concerning Arduino platforms and open source programming, are also given.

Index Terms— security, cryptography, computer architecture, system-on-a-chip, FPGA, ASIC, VLSI design, embedded systems, Arduino.

I. INTRODUCTION

THE spreading revolution of communications, and especially the wireless and mobile applications of them, has created special needs for safe and secure communications [1]. With the adoption of the hardware advantages the center of interest has been moved to cryptographic hardware, regarding implementation aspects, of security primitives [2]. With the term cryptographic hardware, the research community refers to both theoretical and practical adoptions of cryptographic engineering, for a variety of purposes and applications such as: encryption and decryption processors, digital signature systems, key generation and distribution schemes, as well as random number generators [3]. In order to implement efficiently a security system, first the responsible team has to design, to implement, to validate and to test the implementation for the efficient performance of it [2].

This work introduces the aspects of cryptographic hardware and embedded systems, regarding implementation issues, for several aspects of secure communications: block ciphers, hash functions, random number generators, etc. It is also presented future directions, concerning promising hardware devices such as Arduino, and gives aspects of open source programming of them.

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II. DESIGN PROCESS: SYSTEM-ON-A-CHIP

This paragraph is related to the basics of System-On-A-Chip design process, which contains the following sections: SoC design, design flow and design life through specifications [4-6].

A. SoC Design

Let's assume the design of a crypto-processor for a specific purpose like secure satellite communications, which is illustrated in the next Figure 1:

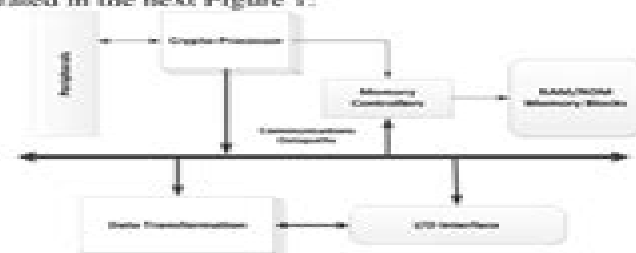


Fig. 1. Crypto-Processor Architecture of a Canonical SoC Design

The main subsystems are: the crypto-processor, the memories sub-blocks (RAM/ROM, memory controllers), I/O interfaces with the external communication systems, units data transformation units, as well as communication datapaths [4]. Such a design, although maybe seemed generic, applies most of the structures and methodologies, that are used in SoC design [5]. The internal subsystems vary in nature and in performance issues. These blocks will be designed developed and specified, during the design process. According to the application needs its time, the above design could be transformed to a more complicated one, which may integrates different interfaces, data transformations, a set of different processors, as well as a number of other peripherals and subsystems like memory units [4].

B. Design Flow

In most of the cases, designers do achieve to meet the requirements of the application design, through two alternative design flows. Regarding ASICs (Application Specific Integrated Circuits), the waterfall model is followed, Fig. 2. According to this model, the design process is divided to seven alternative stages, which can be implemented by

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