

Voltage-controlled oscillators: Inexpensive alternative to analog-to-digital converters

BRIAN PARTRIDGE

Department of Experimental Psychology, University of Oxford, Oxford, England

and

RICHARD DAWKINS and CHARLES AMLANER, JR.

Animal Behaviour Research Group, Department of Zoology, University of Oxford, Oxford, England

We describe a simple software mimic of an analog-to-digital (A/D) converter that is suitable for most laboratory applications requiring A/D. The routine samples output from a voltage-controlled oscillator that can be built for around \$6. Results of proving trials show the output to be linear and sampling rates of up to 50/sec are possible.

A typical analog-to-digital (A/D) converter for a laboratory computer may cost several hundred dollars. We describe here an alternative that is adequate for many biological and psychological applications, but that only costs around \$6 to make. The principle is simple, and the only computer interfacing required is available on most typical laboratory minicomputers, and indeed would be required as part of the interface for a conventional A/D converter. Input voltage to the circuit is used to control the frequency of an oscillator and this frequency is then analyzed by the computer. The reason that the system is so inexpensive is that this analysis is done by software rather than by hardware. The technique has already been used in the "organ" event recording system (Dawkins, 1971). The original paper included a speculative reference to its possible application for analog conversion, but it was not then known whether it was feasible in practice.

The present paper describes an oscillator circuit that is accurate enough to give reliable results and has already given good service in behavioral research (Pitcher, Partridge, & Wardle, 1976; Partridge & Pitcher, Note 1). The system has been tested on a PDP 8 (Digital Equipment Corporation). No doubt modified versions would work on comparable computers. Sample results from proving trials are given, and a version of the program in PDP 8 machine code is included in the Appendix.

CIRCUIT DESCRIPTION

The circuit, shown in Figure 1a, is a free-running square-wave oscillator that has a programmable output frequency dependent on the voltage across Pins 7 and 8. The control voltage may be varied by a potentiometer; in our application, a 10-turn linear 50K potentiometer (Radio Spares Ltd.) allowed us a scale of 2,000 arbitrary units. The circuit produces pulse periods (1/frequency)

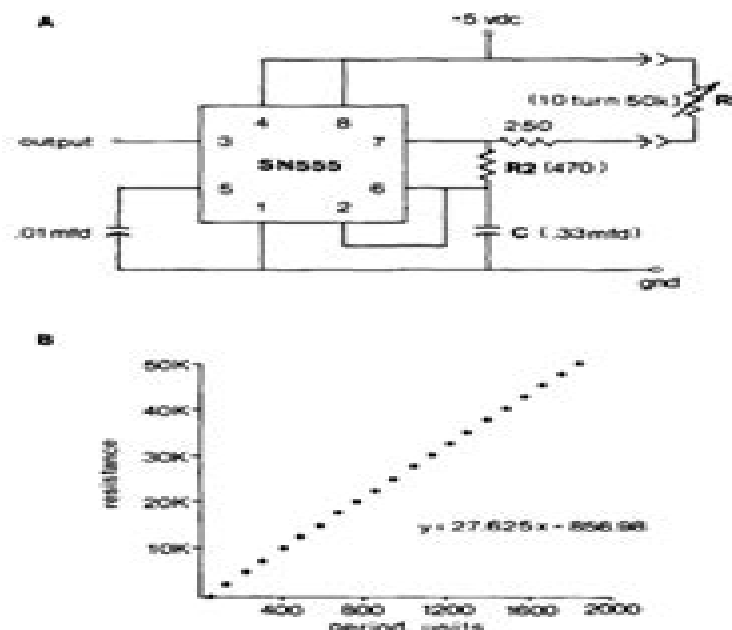


Figure 1. (a) Circuit diagram for voltage-controlled oscillator, using a Signetics 555 timer. R1, R2, and C can be altered (see text) to provide output in the desired range. A single 250-ohm resistor is placed in series with R1 to prevent the resistance across Pins 7 and 8 ever dropping to zero. That would result in output frequency equal to zero, and the computer would hang up, waiting for 10 of the infinitely long pulses. (b) Output from the subroutine ORG as a function of resistance (R1) and our implementation of the circuit. Output will always be linear but individual chips may produce slightly different values for the y-intercept.

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Time-domain Analog-to-Digital Converters using Voltage-Controlled Oscillators SeongHwan Cho,Jaewook Kim,Wonsik Yu,Young-Gyu Yoon,2015-06-24 This book describes time domain analog to digital converters ADCs using voltage controlled oscillators VCOs Unlike conventional ADCs that require precise analog circuits in the voltage domain time domain ADCs use mostly digital circuits that benefit from transistor scaling and therefore are suitable for current and future CMOS processes This book is intended for designers who want to build ADCs with advanced CMOS processes using digital building blocks

VCO-Based Quantizers Using Frequency-to-Digital and Time-to-Digital Converters Samantha Yoder,Mohammed Ismail,Waleed Khalil,2011-08-28 This book introduces the concept of voltage controlled oscillator VCO based analog to digital converters ADCs Detailed explanation is given of this promising new class of high resolution and low power ADCs which use time quantization as opposed to traditional analog based i e voltage ADCs

Linearizing Techniques for Voltage Controlled Oscillator Based Analog to Digital Converters Sachin B. Rao,2013 Voltage controlled oscillator VCO based ADC is an important class of time domain ADC that has gained widespread acceptance due to their several desirable properties VCO based ADCs behave like an open loop continuous time delta sigma modulator and achieve excellent resolution by first order noise shaping the quantization error However the SNDR of an open loop VCO based ADC is severely distortion limited by the voltage to frequency tuning characteristics of the VCO This work examines various techniques that have already been proposed to overcome the VCO tuning non linearity problem Two new VCO based ADC architectures that overcome the limitations of the conventional approaches are proposed In the first approach the ADC is linearized by forcing the VCO to operate at only two operating points using a front end two level modulator With this technique the linearity is improved without using either a multi bit feedback DAC or calibration Fabricated in a 90 nm CMOS process the prototype ADC achieves better than 71 dB SFDR and 59.1 dB SNDR in 8 MHz signal bandwidth while consuming 4.3 mW power The ADC achieves a figure of merit of 366 fJ/conv step which is comparable with other state of the art time based ADCs In the second approach the need for a front end two level modulator is obviated using linearizers which introduce an inverse of VCO's voltage to frequency characteristics in the signal path A deterministic digital calibration unit runs continuously in the background and builds the inverse voltage to frequency transfer function Implemented in a 90nm CMOS process this on chip calibration improves SFDR of the prototype ADC from 46 dB to more than 83 dB The ADC consumes 4.1 mW power and achieves 73.9 dB SNDR in 5 MHz signal bandwidth resulting in an excellent figure of merit of 101 fJ/conv step

Power Efficient Analog-to-digital Converters Using Both Voltage and Time Domain Information Taehwan Oh,2013 As advanced wired and wireless communication systems attempt to achieve higher performance the demand for high resolution and wide signal bandwidth in their associated ADCs is strongly increased Recently time domain quantization has drawn attention from its scalability in deep submicron CMOS processes Furthermore there are several interesting aspects of time domain

quantizer by processing the signal in time rather than only in voltage domain especially for power efficiency This research focuses on developing a new architecture for power efficient high resolution ADCs using both voltage and time domain information As a first approach a new delta sigma ADC based on a noise shaped two step integrating quantizer which quantizes the signal in voltage and time domains is presented Attaining an extra order of noise shaping from the integrating quantizer the proposed delta sigma ADC manifests a second order noise shaping with a first order loop filter Furthermore this quantizer provides an 8b quantization in itself drastically reducing the oversampling requirement The proposed ADC also incorporates a new feedback DAC topology that alleviates the feedback DAC complexity of a two step 8b quantizer The measured results of the prototype ADC implemented in a 0.13 μm CMOS demonstrate peak SNDR of 70.7dB 11.5b ENOB at 8.1mW power with an 8x OSR at 80MHz sampling frequency To further improve ADC performance a Nyquist ADC based on a time based pipelined TDC is also proposed as a second approach In this work a simple V-T conversion scheme with a cheap low gain amplifier in its first stage and a hybrid time domain quantization stage based on simple charge pump and capacitive DAC in its backend stages are also proposed to improve ADC linearity and power efficiency Using voltage and time domain information the proposed ADC architecture is beneficial for both resolution and power efficiency with MSBs resolved in voltage domain and LSBs in time domain The measured results of the prototype ADC implemented in a 0.13 μm CMOS demonstrate peak SNDR of 69.3dB 11.2b ENOB at 6.38mW power and 70MHz sampling frequency The FOM is 38.2fJ/conversion step

Time-to-Digital Converters Stephan Henzler, 2010-03-10 Micro electronics and so integrated circuit design are heavily driven by technology scaling The main engine of scaling is an increased system performance at reduced manufacturing cost per system In most systems digital circuits dominate with respect to die area and functional complexity Digital building blocks take full vantage of reduced device geometries in terms of area power per functionality and switching speed On the other hand analog circuits rely not on the fast transition speed between a few discrete states but fairly on the actual shape of the transistor characteristic Technology scaling continuously degrades these characteristics with respect to analog performance parameters like output resistance or intrinsic gain Below the 100 nm technology node the design of analog and mixed signal circuits becomes perceptibly more difficult This is particularly true for low supply voltages near to 1V or below The result is not only an increased design effort but also a growing power consumption The area shrinks considerably less than predicted by the digital scaling factor Obviously both effects are contradictory to the original goal of scaling However digital circuits become faster smaller and less power hungry The fast switching transitions reduce the susceptibility to noise e.g. flicker noise in the transistors There are also a few drawbacks like the generation of power supply noise or the lack of power supply rejection

Time-interleaved Analog-to-Digital Converters Simon Louwsma, Ed van Tuijl, Bram Nauta, 2010-09-08 Time interleaved Analog to Digital Converters describes the research performed on low power time interleaved ADCs A detailed theoretical analysis is made of the time interleaved Track Hold since it must be capable of

handling signals in the GHz range with little distortion and minimal power consumption Timing calibration is not attractive therefore design techniques are presented which do not require timing calibration The design of power efficient sub ADCs is addressed with a theoretical analysis of a successive approximation converter and a pipeline converter It turns out that the first can consume about 10 times less power than the latter and this conclusion is supported by literature Time interleaved Analog to Digital Converters describes the design of a high performance time interleaved ADC with much attention for practical design aspects aiming at both industry and research Measurements show best inclass performance with a sample rate of 1.8 GS/s, 7.9 ENOBs and a power efficiency of 1 pJ/conversion step

Voltage-controlled Oscillators Brian Partridge, 1978 We describe a simple software mimic of an analog to digital A/D converter that is suitable for most laboratory applications requiring A/D The routine samples output from a voltage controlled oscillator that can be built for around 6 Results of proving trials show the output to be linear and sampling rates of up to 50/sec are possible

Wide-Bandwidth High Dynamic Range D/A Converters Konstantinos Doris, Arthur H.M. van Roermund, Domine Leenaerts, 2006-01-12 IGH SPEED Digital to Analog D/A converters are essential components in digital communication systems providing the necessary conversion of signals encoding information in bits to signals encoding information in their amplitude vs time domain characteristics In general they are parts of a larger system the interface which consists of several signal conditioning circuits Dependent on where the converter is located within the chain of circuits in the interface signal processing operations are partitioned in those realized with digital techniques and those with analog The rapid evolution of CMOS technology has established implicit and explicit trends related to the interface and in particular to the D/A converter The implicit relationship comes via the growth of digital systems First it is a global trend with respect to all interface circuits that increasing operating frequencies of digital systems place a similar demand for the interface circuits The second trend takes place locally within the interface Initially the D/A converter was placed at the beginning of the interface chain and all signal conditioning was implemented in the analog domain after the D/A conversion The increasing flexibility and robustness of digital signal processing shifted the D/A converter closer to the end point of the chain where the demands for high quality high frequency operation are very high

Voltage to Frequency Converter for Integration in Time Domain Induced Polarization Receiver David G. Kissinger, 1977

Integrated Voltage Controlled Oscillators Using Large Time Constant Distributed Parameter Phase Shift Networks Hans Helmut Stellrecht, 1968

Amplifier-based Analog-to-digital Converters Using Time-domain Signal Processing [1], 2015

Efficient Use of Time Information in Analog-to-digital Converters Yue Hu, 2014 Time domain data conversion has recently drawn increased research attention for its highly digital nature in favor of process technology scaling Also as the time information being carried by binary voltage time domain operation is much less sensitive to voltage noise compared to conventional voltage domain operation However for analog to digital converter ADC application the challenge lies in the methodology of benefiting from time domain

operation while maintaining improving the overall data conversion accuracy and power efficiency This dissertation has a focus on the investigation of novel data conversion topologies based on classic voltage domain operation that is capable of generating time information to improve ADC resolution system stability and speed without power penalty In the first approach a novel continuous time CT delta sigma modulator DSM using a time interleaved quantizer is proposed and implemented Along with the doubled sample rate the proposed architecture utilizes time information to perform correlated coupling between the two quantizer channels A 120MS s CT delta sigma ADC using proposed technique is implemented in 0 18 micro m CMOS process The measurement results achieve second order noise coupling from the interleaved quantizer itself without extra phases More importantly excess loop delay of two full sample clocks is compensated by time domain signal coupling the resulted CT DSM is fully stabilized in 120MHz sampling rate and achieves 11 effective number of bits ENOB In the second approach a new category of pulse width modulation PWM scheme is proposed and described time symmetric PWM TSPWM An ADC structure is further proposed and implemented utilizing this novel voltage to time converter followed by a first order noise shaped switched ring oscillator SRO TDC quantizer This ADC topology takes advantage of the TDC speed scaling for its digitized operation to boost the overall ADC resolution and signal bandwidth while the voltage to time front end is able to remain at a much lower speed than the TDC thanks to the proposed technique This is the first work that decouples the PWM modulation rate from TDC quantizing speed without distortion penalty Built in 0 18 micro m the implemented ADC is able to sample at a range from 20MHz to 40MHz the generated pulse train is quantized by the following SRO TDC at a rate of 400MHz The prototype chip shows a SFDR improvement over 24dB on the ADC output when TSPWM is used

Design of a Voltage-to-time Converter and Selection of a Time-to-digital Converter for Use in a Time-based Analog-to-digital Converter Peter A. Osheroff,2015 **Design of Voltage Controlled Oscillators** Monika Bhardwaj,2011-11 *High Frequency Wideband Temperature Stable Voltage Controlled Oscillators* Wei-Lien Yang,1995 Millimeter-wave Voltage-controlled Oscillators and Frequency Doubler Yu-Ju Chuang,2004 *Time-based Noise-shaping Techniques for Time-to-digital and Analog-to-digital Converters* Brian LeRoy Young,2013 In this dissertation time based signal processing techniques and their applications in oversampling and noise shaping data converters are examined These techniques demonstrate the ability to shift the burden of high performance analog circuits from the compressed voltage domain to the augmented time domain First the potential of high order noise shaping and phase domain feedback in time to digital converters TDCs is explored A prototype phase reference second order continuous time delta sigma TDC for sensor applications was fabricated in 90nm CMOS and achieves 64 dB dynamic range in 1MHz signal bandwidth Second an ultra high performance oscillator based delta sigma modulator architecture is investigated The proposed circuit is a third order continuous time PLL Based Delta Sigma Modulator with simulated 77 dB SNDR in 40MHz signal bandwidth with OSR of 16 and is fabricated in 65nm CMOS

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